Parallelisation of Digital Systems Processing Arbitrarily Sampled Signals

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Abstract — For the first time systems which process arbitrarily sampled signals are parallelised with a selectable degree of parallelisation where a graphical representation is used. To illustrate the presented parallelisation method, it is applied to the Farrow-structure used for arbitrary sampling rate conversion.

1 INTRODUCTION

In order to realise digital SISO(Single-Input-Single-Output)-systems to be operated at clock speeds beyond technological feasibility, these systems have to be replaced with equivalent MIMO(Multiple-Input-Multiple-Output)-systems (Fig. 1). Hence, the subsystems of the latter can be operated at lower speed.

2 GRAPHICAL PARALLELISATION METHOD

The derivation of the equivalent MIMO-system is subdivided into three steps:

1. Each basic element of the SISO-system is parallelised separately. To this end, each of these elements is cascaded with an SP(serial-to-parallel)- and its complementary PS(parallel-to-serial)-interface with an unit overall transfer function (cf. Fig. 5, grey box). Thereafter the basic element is shifted between the SP- and PS-interfaces by exploiting the graphical equivalences.

2. The resulting parallelised subsystems are connected according to the structure of the SISO-system.

3. Finally the intermediate PS- and SP-interfaces between the cascaded subsystems are eliminated by replacing them with direct connections leaving only the SP-interface at the input and the PS-interface at the output of the overall system (Fig. 4).

As a consequence of this parallelisation method, SP- and PS-interfaces with suitable up- and downsamplers for processing arbitrarily sampled signals have to be defined (sec. 2.1). In compliance with these new elements novel graphical equivalences have to be derived: Here solely the most essential graphical equivalence is presented which enables the elimination of cascaded PS- and SP-interfaces (cf. step 3). Finally, the most essential basic elements for the Farrow-structure are parallelised in section 2.2.

2.1 New Elements [4]

A generalised downsampler (Fig. 2, left) transfers its input signal in an unscaled and delay-free manner
to its output at the output time instants $t_o$:
\[
y(t_o) = x(t_i) \quad \forall \; t_i = t_o. 
\]
(1)

To this end, $t_o$ has to be a subset of the input time instants $t_i$, whereas $t_i$ can be any set of arbitrary time instants.

\[
x(t_i) \quad y(t_o) \quad x(t_i) \quad y(t_o)
\]

Figure 2: Generalised down- and up-sampler

The output samples $y(t_o)$ of a generalised up-sampler (Fig. 2, right) are identical to its input samples $x(t_i)$ and zero for all $t_o \neq t_i$:
\[
y(t_o) = \begin{cases} x(t_i) & \forall \; t_o = t_i, \\ 0 & \text{otherwise.} \end{cases} 
\]
(2)

Hence, $t_i$ is a subset of $t_o$, whereas $t_o$ can be any set of arbitrary time instants. Note that the transposition of a generalised up-sampler yields a generalised down-sampler where the input sampling grid is not indicated in Fig. 2, left.

\[
x(t_i) \quad y(t_o) \quad x(t_i) \quad y(t_o)
\]

Figure 3: Generalised SP-interface (left) and PS-interface (right)

For the decomposition (interleaving) of an arbitrarily sampled signal a generalised SP-interface (PS-interface) consisting of $P$ generalised down-samplers (upsamplers) is needed, with $P$ being the degree of parallelisation (Fig. 3). To this end, the set $t_i$ ($t_o$) of input (output) sampling instants jointly represented by $t_{i,o}$ is divided into $P$ subsets according to
\[
t_{i,o} = t'_{0} \cup t'_{1} \cup \cdots \cup t'_{p-1} \quad \text{and} \quad t'_{l} \cap t'_{m} = \emptyset, l \neq m. 
\]
(3)

In the following, the special case $t'_{p} = t_{i,o}(Pk + p)$, $k \in \mathbb{Z}$ and $p \in [0, \ldots, P - 1]$, is applied which leads to a simplified system control.

\[
x(t_i) \quad y(t_o) \quad x(t_i) \quad y(t_o)
\]

Figure 4: Elimination of interfaces

2.2 Parallelisation of Basic Elements

The basic elements of a system processing arbitrarily sampled signals are the summation and distribution nodes, multiplications with constant and time-varying coefficients, arbitrary delays and generalised down- and up-samplers. The parallelisation of the first three basic elements is straightforward, whereas the parallelisation of the remaining basic elements is presented subsequently except for the generalised up-sampler (cf. [4]).

\[
x(t_i) \quad y(t_o) \quad x(t_i) \quad y(t_o)
\]

Figure 5: Parallelisation of multiplication with time-varying coefficient

A cascade of a PS- and a SP-interface is depicted in Fig. 4. Assuming the same sampling instants $t'_p$, $p \in [0, \ldots, P - 1]$, for both up- and down-samplers, the cascade can be replaced by a bunch of direct connections.

\[
x(t_i) \quad y(t_o) \quad x(t_i) \quad y(t_o)
\]

Figure 5: Parallelisation of multiplication with time-varying coefficient
The arbitrary delay $z^{-\beta \alpha}$ can only be shifted between the SP- and PS-interfaces if the sampling instants of the generalised upsamplers are changed from $t'_{p}$ to $t'_{p} + \beta T_{\alpha}$ (Fig. 6).

In the parallelised downsampler the task of downsampling is distributed over $P$ branches by dividing the sampling instant set $t_{o}$ into $P$ subsets according to (3) (Fig. 7).

3 PARALLELISATION OF FARROW-STRUCTURE

The Farrow-structure is an efficient implementation of the polynomial-based approximation method for arbitrary sampling rate conversion [1, 6]. For the calculation of each output sample $y(t_{o})$ a set of $\eta$ input samples $u(\lambda T)$ is selected. This set consists of $(\lambda_{-} + 1)$ current/past and $\lambda_{+}$ future input samples where the index $\lambda_{0} \in \mathbb{Z}$ of the current input sample is given by

$$\lambda_{0} = \left\lfloor \frac{t_{v}}{T} \right\rfloor.$$

Hence, $t_{v}$ can be represented by $\lambda_{0}$ and the normalised inter-sample position $\Delta$:

$$t_{v} = \lambda_{0} T + \Delta T, \text{ with } \Delta = \frac{t_{v}}{T} - \lambda_{0}. $$

For a parallelisation of the Farrow-structure a novel signalflow graph description is required which includes system control (Fig. 8). To this end, the generalised downsamplers and the delays $z^{-\eta+1+p}$ and $z^{-\Delta T}$ are introduced. The selection of the $\eta$ input samples is carried out by the generalised downsamplers. The delays $z^{-\eta+1+p}$ guarantee that all input samples are available at the same time instant $(\lambda_{0} + \lambda_{+})T$ for subsequent signal processing. The delays $z^{-\Delta T}$ ensure the correct time relation between the output samples. Due to the extra delay of $\lambda_{+} T$ the calculation of $y'(t_{v})$ is not performed at $t_{v}$ but at $t_{o} = (t_{v} + \lambda_{+} T): y(t_{o}) = y'(t_{v})$.

For the parallelisation of the Farrow-structure the graphical method of section 2 is applied to the Farrow-structure depicted in Fig. 8 utilising the parallelised basic elements of section 2.2. The result is depicted in Fig. 9 where all shaded PS- and SP-interfaces are eventually replaced with a bunch of direct connections according to Fig. 4.

Since $P$ output values $y(t_{o})$ are calculated in $P$ parallel branches alternately, the minimum execution time is extended to at least $P \min \{ t_{o}(i + 1) - t_{o}(i) \}$, where $t_{o}(i)$ and $t_{o}(i+1)$ are the $i$-th and $(i+1)$-th output sampling instant, $i \in \mathbb{Z}$. Hence, $P$ can be selected appropriately to achieve technical feasibility even for high output rates.
4 CONCLUSION

The graphical parallelisation method was extended to systems processing arbitrarily sampled signals. Subsequently, it was applied to the FARROW-structure (Fig. 9).

The completely parallelised system can be utilised in case of out- and input rates beyond technological feasibility. Note that the parallelised structure requires a greater chip area and complexer system control.

In case of an acceptable input rate but technologically infeasible output rate only the subsystem consisting of the delays $z^{-\Delta T}$ and the time-varying coefficients $\Delta$ has to be parallelised.

References


