Polyphase Realisation of Fractional Sample Rate Converters

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Abstract

The polyphase approach to synchronous fractional sample rate conversion by \( L/M \), where \( L, M \) are co-prime integers, is revisited. In contrast to existing publications [1-5], a rigorous, systematic and yet straightforward derivation of an optimum causal implementation is deduced.

1 Introduction

A particular and important case of the omnipresent need of sample rate alteration in digital signal processing is the conversion of the sampling rate by a noninteger factor \( L/M \), where \( L \) and \( M \) are positive, relatively prime integers. The system theoretic approach to fractional sample rate alteration is characterised by the cascade connection of an interpolator for \( L \)-fold rate increase followed by a decimator for \( M \)-fold rate reduction [1,2] according to Fig.1, where the interpolator and decimator filters have merged in one filter \( H(z) \). Here, all filter operations have to be performed at the highest rate \( F = 1/T \) (\( T \): Sampling period), which is related to the system input rate \( F_i \) and output rate \( F_o \) in a synchronous manner by

\[
F = LF_i = MF_o
\]  

Figure 1: System theoretic approach to fractional sample rate conversion (FSRC)

As a result, the \( z \)-domain representations of the input and output signals of Fig.1 are related to the respective input and output sampling rates [1,2] according to

\[
z_i = e^{sT_i} = e^{sTL} = z^L \quad \text{and} \quad z_o = e^{sT_o} = e^{sTM} = z^M
\]  

By suitably decomposing the highly inefficient structure of Fig.1 into polyphase components, it is possible to perform all arithmetic operations at the subnyquist rate

\[
F_s = \frac{F}{LM} = \frac{F_i}{M} = \frac{F_o}{L} \iff z_s = e^{sTL} = z^{LM}
\]  

A heuristic derivation of this approach is given in [1,2]. An optimum polyphase structure of a fractional sample rate converter was disclosed in a US-patent [3] and two conference papers [4,5], respectively. This approach requires one input commutator for \( M \)-fold decimation, and one output commutator for \( L \)-fold sample interleaving. All operations (including memory shift) are performed at the subnyquist rate \( F_s \). In [3-5], however, a proper step-by-step derivation of this polyphase structure is missing. Hence, a rigorous, systematic derivation of an optimum polyphase realisation of the above defined fractional sample rate converter (FSRC) is developed subsequently.

2 An Optimum Polyphase Realisation

Starting from Fig.1 let

\[
H(z) = z^{-\lambda} H_c(z), \quad \lambda \in \mathbb{N}_0
\]  

where \( H_c(z) \) represents a causal, possibly minimum phase FIR or IIR filter. Due to the extra memory, \( H(z) \) is no longer minimum phase but still causal and, hence, realisable.

The derivation of the optimum FSRC realisation is subdivided into five steps. In Step 1, the FSRC filter \( H(z) \) is decomposed into polyphase components, where subsequently always type 1 polyphase decomposition [1] is applied. In Step 2, the sequential order of these polyphase components is systematically rearranged, such that the noble identities [1] can readily be exploited in Step 3. In Step 4, each original polyphase component is subjected to a second polyphase decomposition, thus yielding an optimum FSRC structure: Blocking the input signal into a length-\( M \) vector-valued signal, which is the input to a multiple-input multiple-output (MIMO) linear time-invariant (LTI) system producing a length-\( L \) vector-valued signal at its output that, subsequently, is unblocked to form the output signal. Finally, the optimum
polyphase realisation with one input and one output commutator each is presented in Step 5.

Polyphase decomposition is straightforward for FIR filters [1, 2] whereas, in general, a standard IIR filter transfer function must be subjected to an equivalence transformation before polyphase decomposition can be applied [6].

**Step 1: Polyphase Decomposition of** \( H_c(z) \)**

In the derivation procedure we start, for instance, with an \( L \)-branch polyphase decomposition of the FSRC filter [1, 2]:

\[
H(z) = z^{-\lambda} \sum_{l=0}^{L-1} z^{-l} H_l(z^L) \quad (5)
\]

**Step 2: Systematic Rearrangement of Sequential Order of Polyphase Components according to (5)**

The first polyphase decomposition (5) is rearranged by mapping of the summation index \( l \) according to

\[
l := (l M) \mod L = l M - p_l L \quad (6)
\]

where \( l = 0, 1, \ldots, L-1, p_l \in \mathbb{N}_0 \) and \( 0 \leq p_l \leq p_{L-1} \). This substitution represents a one-to-one mapping on \( \{0, 1, \ldots, L-1\} \) since \( L \) and \( M \) are coprime. Upper and lower bounds of \( p_{L-1} \) are readily deduced from (6) using the fact that \( l = 0 \) is definitely related to \( p_0 = 0 \), limiting the remaining mapped indices to \( 1 \leq (l M)_L \leq L-1 \). Introducing \( l = L-1 \) into these inequalities in conjunction with the right hand side of (6), yields the upper bound of \( p_{L-1} \in \mathbb{N} \):

\[
p_{L-1} = \left[ \frac{(L-1)M-1}{L} \right] \quad (7)
\]

where \( 0 \leq x - \lfloor x \rfloor < 1 \). By introducing the index mapping (6) into (5) and by setting in compliance with (7)

\[
\lambda = p_{L-1} L \quad (8)
\]

we get

\[
H(z) = z^{-p_{L-1} L} \sum_{l=0}^{L-1} z^{-((l M - p_l) L)} H_{(l M)M}(z^L)
\]

\[
= \sum_{l=0}^{L-1} z^{-l M} E_l(z^L) \quad (9)
\]

where the quantities

\[
E_l(z^L) = H_{(l M)M}(z^L) z^{-(p_{L-1} - p_l) L} \quad (10)
\]

represent the reordered components of the \( L \)-branch polyphase decomposition of the FSRC filter \( H(z) \), as depicted in Fig.2.

**Step 3: Application of Noble Identities [1]**

The structure obtained so far by decomposition of \( H(z) \) according to (9) and Fig.2 represents a polyphase input interpolator of the FSRC with subsequent decimation by \( M \), such that all \( L \) branch filters (10) receive identical input signals expanded by \( L \) [1, 2]. Next, by applying the noble identities [1] to the branch filters and the output delay chain of (9) being composed of delays that are multiples of \( z^{-M} \), the input expander and the output decimator are shifted into the decomposed FSRC polyphase filter until they are directly cascaded at the output of each polyphase branch filter. Reversing the sequential order of the expander-decimator cascade, as justified in [1], results in the transformed structure as shown in Fig.3. The associated polyphase representation, derived from (9), is given by

\[
H(z) = \sum_{l=0}^{L-1} z^{-l M} E_l(z^L) = \sum_{l=0}^{L-1} z^{-l M} E_l(z_i) \quad (11)
\]
where the \(z\)-domain variables are related to the operating sampling rates according to (2).

\[
H(z) = \sum_{l=0}^{L-1} z^{-l} E_l(z_i) = \sum_{l=0}^{L-1} z^{-l} \sum_{m=0}^{M-1} E_{lm}(z_s) z^{-m}
\]  

(12)

Again, this representation is related to the actual sampling rates used for filtering \(F_s\), blocking \(F_i\) and unblocking \(F_o\) operations, as defined by (3).

**Step 5: Commutator Polyphase Structure**

In Fig.5 the 1-to-\(M\) input blocking and the \(L\)-to-1 unblocking circuits of Fig.4 are replaced by commutators rotating counterclockwise as appropriate [1,2]. Furthermore, the detailed structures of the MIMO system \(S(z_s)\), resulting from the described twofold polyphase decomposition, is revealed. The corresponding FSRC representation is given by (12).

3 Example

With \(L = 3\), \(M = 5\) and the canonical, causal filter

\[
H_c(z) = \sum_{k=0}^{14} h_k z^{-k}
\]  

(13)

we have chosen a simple FIR example to gain maximum insight. Since the filter length \(N = 15\) is set equal to the number of branches \(L \times M = 15\) (cf.
Fig. 5, each path is provided with just one non-zero coefficient by the twofold polyphase decomposition process. From (7) and (8) follows $p_2 = 3$ and $\lambda = 9$, corresponding to the short extra delay of $9T = 3T$. The index mapping (6) of the first polyphase decomposition yields

\[
\begin{align*}
l &\quad 0 \quad 1 \quad 2 \\
p_l &\quad 0 \quad 1 \quad 3 \\
(lM)_L &\quad 0 \quad 2 \quad 1
\end{align*}
\]
resulting in the assignment defined by (10) in conjunction with (2) and (5)

\[
\begin{align*}
E_0(z_i) &= z_i^{-3} H_0(z_i) = z_i^{-3} \sum_{k=0}^{4} h_{3k} z_i^{-k} \\
&= \sum_{k=0}^{7} e_{0k} z_i^{-k}; \quad e_{00} = e_{01} = e_{02} = 0 \\
E_1(z_i) &= z_i^{-2} H_2(z_i) = z_i^{-2} \sum_{k=0}^{4} h_{3k+2} z_i^{-k} \\
&= \sum_{k=0}^{6} e_{1k} z_i^{-k}; \quad e_{10} = e_{11} = 0 \\
E_2(z_i) &= H_1(z_i) = \sum_{k=0}^{4} h_{3k+1} z_i^{-k} \\
&= \sum_{k=0}^{4} e_{2k} z_i^{-k}
\end{align*}
\]

In the second decomposition process the quantities $E_l(z_i), l = 0, 1, 2,$ are additionally decomposed into $M = 5$ polyphase components each in a straightforward manner. The ultimately obtained signal flow graph of the optimum fractional sample rate converter (=3/5-decimator) is depicted in Fig. 6.

4 Conclusion

An alternative but for the first time systematic and rigorous derivation of an optimum realisation of the synchronous $L/M$ sample rate converter, with $L, M \in \mathbb{N}$ being relatively prime, has been given. Its merits are: i) All multiplications and additions with zero terms are avoided, ii) all operations (multiplications, additions, delays) are performed at a clock rate ranging both below the input and output rates of the FSRC, and iii) parallel processing is achieved by means of one input commutator for decimation by $M$, and one output commutator for interleaving of $L$ polyphase sequences.

Note that the decomposition procedure of the developed optimum FSRC started with an $L$-branch polyphase decomposition of the input interpolator. Similarly, we could also have started with the polyphase decomposition of the output decimator for rate reduction by $M$. Both approaches and their features will be compared with each other in a forthcoming extended paper.

References


