This paper reports on the specification, analysis and design of a digital 16-slot tree-type FDM demultiplexer for processing of complex-valued signals. The single-chip ASIC to be developed shall eventually be used for mobile satellite communications in a space-borne beamforming environment. The analysis of the linear-phase finite impulse response DEMUX-BFN system includes aliasing due to sample rate reduction, quantisation and clipping noise distortion.

As a result an overall signal-to-distortion ratio of better than 33 dB is obtained at the output port of a 10-element beamforming network with nulling capability. This is achieved with identical DEMUX filter cells of length 11 and an intercell signal wordlength of 8 bit. The optimised filter coefficients are represented by the canonical signed digit code most suitable for VLSI implementation.

Keywords: FDM demultiplexer, beamforming, complex DSP, tree structure, system analysis

1. Introduction

The feasibility of using digital beamforming within an advanced geostationary European land mobile satellite system was investigated under ESA contract [1] most recently. Potential advantages offered by digital beamforming are in terms of usage of on-board power and available spectrum and in flexibility in meeting changing traffic requirements.

The system is assumed to support private networks, each typically comprising a single fixed VSAT terminal and a group of vehicles. Systems providing up to 7000 channels (duplex pair) have been considered with channels typically characterised by 4.8 kbit/s QPSK vocoded voice with 5 kHz channel spacing. The Ku-band feeder link involves one or a few beams whilst the L-band mobile link involves multiple spot beams.

The preferred system configuration is transparent and characterised by agile beams (two-dimensional steering) carrying a single channel per beam such that the maximum beam gain may be obtained in the direction of the mobile. Frequency reuse was considered mandatory on the mobile link.

A key feature of the preferred payload architecture is combined SAW Chirp Fourier Transform (ITG) as a co-author of a survey of digital transmultiplexing. Dr. Gockler is a member of the German Informationstechnische Gesellschaft (ITG) and the European Association for Signal Processing (EURASIP).

In 1988 he received the ITG paper award (Preis der ITG) as a co-author of a survey of digital transmultiplexing.

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Array Antenna

- \( N_E \) 1
- \( N_C \): 1000/7000 QPSK-signals
- \( M_F \)-fold frequency usage
- From MES (10dB fade)

**DEMUX input:**
- 8 bit (I/Q) optimally used
- all channels at maximum power level
- \( P_{sw} = 2 \cdot M_F \cdot 16P = 96P \) (non-coherent)
- \( M_F = 3 \) (fold usage of a frequency)

**Fig. 1.** Return link system configuration; \( i \in [1,N_E] \): element number (antenna); \( k \in [1,L] \): slot number (DEMUX); \( m \in [1,M_F] \): channel number (BFN).

(CFT) [2] and digital processing for individual FDM demultiplexing and multiplexing. This is considered the most flexible and mass/power efficient approach for channelisation [1]. Other features of the overall system are shown in Fig. 1 (return link from mobile to fixed Earth station), and Table 1 [1]. It may be noted that much of the processing scales with the number of array elements.

For the outlined system a digital 16-slot FDM demultiplexer for complex-valued input and output signals is currently being developed as a single-chip VLSI circuit (ASIC) in CMOS technology under ESA contract [3]; DEMUX blocks shadowed in Fig. 1. Although the ASIC is to be integrated into a laboratory demonstrator of agile beamforming by digital means, design rules for future production of radiation hard devices will be considered from the very beginning.

In a preceding study [4] various linear-phase finite impulse response approaches to digital demultiplexing of complex-valued FDM slot-signal were investigated. The tree-structure (or hierarchical multistage method) according to Fig. 2 turned out to be the most promising approach in terms of computational burden (low power consumption) and modularity (suitability to VLSI and testability). Therefore, the tree-DEMUX (disclosed in detail in [4–6]) was adopted as the baseline architecture for this project [3]. For convenience the signal flow graph of one block of Fig. 2 is recalled in Fig. 3: Universal directional filter cell (UNDIFICE). Note oversampling by two (Fig. 2b; [4,5]) according to:

\[
f_{\text{fil}} = 2LB
\]
Table 1
System parameters [1]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Orbital position:</td>
<td>Geostationary at 10°E.</td>
</tr>
<tr>
<td>Service area:</td>
<td>Western Europe, Eastern Europe (to 50°E), Middle East and North Africa. The area is approximately 10°EW by 6°NS from geostationary orbit.</td>
</tr>
<tr>
<td>Channel spacing:</td>
<td>5 kHz</td>
</tr>
<tr>
<td>System capacity:</td>
<td>operational: 7000 channels (duplex pair); preoperational: 1000 channels.</td>
</tr>
<tr>
<td>Frequency band:</td>
<td>Ku-band feeder, L-band mobile. Bandwidth allocation for land mobile is 7 MHz necessitating frequency re-use (spatial).</td>
</tr>
<tr>
<td>Multiple access:</td>
<td>FDMA/FDM for both forward and return links.</td>
</tr>
<tr>
<td>Data rate and modulation:</td>
<td>4.8 kbit/s QPSK has been assumed as a baseline (vocoded voice).</td>
</tr>
<tr>
<td>Link performance:</td>
<td>End to end C/No of 45 dBHz corresponding to BER of $10^{-4}$.</td>
</tr>
<tr>
<td>Fade margins:</td>
<td>10 dB on mobile link, 3 dB in feeder link.</td>
</tr>
<tr>
<td>Mobile link antenna:</td>
<td>Phased array with diameter in the range of 4 to 12 m (corresponding beamwidth in the range 3.27° to 1.09°). Multiple spot beams.</td>
</tr>
<tr>
<td>Fixed earth stations:</td>
<td>VSAT type with 1.75 m diameter antenna, 10 watts transmit power and 400°K receive noise temperature.</td>
</tr>
<tr>
<td>Mobile terminals:</td>
<td>10 dB gain for terminals equipped for telephony, 4 watts transmit power and 300°K noise temperature.</td>
</tr>
<tr>
<td>Mission lifetime:</td>
<td>10 years</td>
</tr>
</tbody>
</table>

where $f_s^1$: DEMUX input sampling rate, $L = 16$: number of usable frequency slots and $B$: frequency slot spacing ([3]: $B \geq 10$ kHz).

The objective of this paper is to report on the design of a digital 16-slot (i.e. 4-stage) tree-type FDM DEMUX, as shown in Figs. 2 and 3, which shall be part of the multiple beamforming network (BFN) of Fig. 1. All parameters are determined via a thorough model-based analysis of the DEMUX-inherent deteriorations considering the impact of the envisaged single-chip ASIC implementation. To fully benefit from the modularity of the DEMUX architecture all UNDICEs are assumed identical; Figs. 2 and 3.

In section 2, system performance is specified according to [3], and basic assumptions for system analysis are stated. System analysis (section 3) takes into account aliasing (spectral foldover due to sample rate decimation) and quantisation noise complicant with [4,5] and, in addition, clipping noise due to overflow saturation. In section 4, all DEMUX parameters are determined by applying the results of system analysis. Finally, system design is verified by simulation.

2. Specification of DEMUX

In compliance with [3], the performance of the digital 16-slot DEMUX is indirectly specified by the signal-to-distortion ratio SDR at the output port of the BFN, assuming the complex-valued input signals of the DEMUXes being corrupted only by quantisation noise due to rounding to $w_F = 8$ bit; Fig. 1. (Note that all signal-wordlengths are understood to include sign.) Provided that:
- each frequency slot contains $M_F = 3$ spatially disjoint co-channels, nominally all at the same frequency but non-coherent with each other
- the 8-bit input and output data words of each DEMUX are used in an optimum manner (calling for appropriate demultiplexer scaling)
- the total out-of-band power of partially attenuated slot signals (which is due to oversampling by two) equals the in-band power of the 16 desired slots
- all channels are at their maximum power levels (corresponding to 0 dB fade condition)

The signal to distortion ratio of any channel is specified at the BFN output port by [3]:

$$\text{SDR} \geq 33 \text{ dB}$$  \hspace{1cm} (2)

assuming that:

- $N_E = 10$ DEMUX output sequences are combined in the BFN
- signals ($P_0$) and aliasing contributions ($N_A$) of different DEMUXes combine coherently
- quantisation ($N_Q$) and clipping ($N_C$) noise of different DEMUXes combine non-coherently

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Fig. 3. Universal directional filter cell (UNDIFICE); $c_i = \mu h_i$, except for $c_0 = \mu h_0 N2$; $h_i$ : real coefficients of halfband prototype.
- all undesired co-channels in the considered slot are exactly nulled by spatial filtering [1]
- partial attenuation of aliasing contributions (being not co-channel) by spatial filtering is accounted for by the BFN misadjustment factor $M_F^2 = 2$.

Thus:

$$SDR = 10 \log_{10} \frac{P_0}{N_A + N_D + N_C}$$  \hspace{1cm} (3)$$

where all quantities are related to BFN output port and considered band-limited to slot bandwidth $B$.

To determine $P_0$ of (3) the complex-valued channel signals (QPSK [1]) are modelled by complex sinusoids $a_{lm} e^{2\pi j k T}$ of identical amplitudes $a_{lm} = a$. Then the overall input power to each DEMUX is given by:

$$P_F = 2 L M_F^2 P = 2 L M_F^2 a^2 = P_R + P_I$$  \hspace{1cm} (4)$$

in accordance with the above specifications ($P$: power of complex signal in one channel). In addition $P_R = P_I = P_F/2$ is assumed, where $P_R$ and $P_I$ represent the power of the real and the imaginary parts of the FDM input signal.

At the input and output ports of all UNDIFICEs overflow saturation by $\pm 1 (S_1)$ is anticipated. Introducing identical parametric peak factors $p_f$ for the real and imaginary components of the complex FDM input signal, we require:

$$p_f \sqrt{P_R} = p_f \sqrt{P_I} = S_1 = 1$$  \hspace{1cm} (5)$$

Rearranging (5) in conjunction with (4) results in:

$$a = \frac{1}{p_f \sqrt{L M_F^2}}$$  \hspace{1cm} (6)$$

Applying the same procedure and the same peak factor $p$ to the DEMUX output signals yields the identical amplitudes $b$ of the processed model sinusoids:

$$b = \frac{1}{p_f \sqrt{M_F^2}}$$  \hspace{1cm} (7)$$

From (6) and (7) the common UNDIFICE scale factor readily follows:

$$\gamma = (b/a)^{1/4} = L^{1/8} = \sqrt{2}$$  \hspace{1cm} (8)$$

guaranteeing identical power levels at the input and output ports of each UNDIFICE. Note that the $M_F$ signals in the contiguous DEMUX output slot (cf. Fig. 2b: $f/f^0_E \in [0.5,1]$) are multiply aliased.

Due to coherent superposition of both signals and aliasing contributions and the nulling property of the BFN, the total BFN output power is given by:

$$P_B = N_E^2 (1 + M_F^2) b^2 = \frac{N_E^2}{p_f^2} \frac{1 + M_F^2}{M_F}$$  \hspace{1cm} (9)$$

where use is made of (7). Part of it, the power $P_0$ of the desired channel (B)

$$P_0 = N_E^2 b^2 = \frac{N_E^2}{p_f^2} \frac{1}{M_F}$$  \hspace{1cm} (10)$$

has to be introduced into (3).

For precaution, clipping at $\pm 2 (S_3)$ is foreseen after BFN weighting (Fig. 1: $|y_{lim}| \leq 2$). Furthermore, an appropriate saturation level $S_3$ has to be introduced at BFN output port. Assuming again the same peak factors $p_f$ as before for the real and the imaginary BFN output components of power $P_B/2$ according to (9), from $p_f \sqrt{P_B/2} = S_3$ the resulting saturation level of:

$$S_3 = N_E \sqrt{\frac{1 + M_F^2}{2M_F}} = 7.07$$

readily follows. For practical reasons the BFN output overflow is more conservatively saturated by $\pm 8 (S_3)$ consistent with (9). As a consequence of $S_3 > S_3$, at the BFN output port no overflow is expected.

3. System analysis

The various deteriorations $N$ of the DEMUX-BFN system contributing to the denominator of (3)
are indicated in Fig. 4. Subscript A refers to aliasing, subscripts i, F, B and m to quantisation and subscript C to clipping.

First, the complex-valued input signal to the DEMUX is quantised component-wise to \( w_F \) bits. Due to saturation level \( S_1 \) quantisation not only occurs at the rear but (sometimes) also at the front end of the respective sample. Source signal quantisation is the same as output quantisation of each of the four cascaded UNDIFICEs in each signal path of any slot.

Next, in each UNDIFICE an aliasing contribution \( (N_A) \) and some quantisation noise \( (N_i) \) is produced. Aliasing can only occur in conjunction with decimation, where non-ideally rejected spectral portions are folded onto the useful spectrum. This may readily be understood from considering the passband and stopband of the spectral representation of Fig. 2 (see also [4–6]). UNDIFICE internal quantisation noise contribution is due to re-quantisation after each multiplication; Fig. 3. Note that additional overflow bits are foreseen after the summing points such that intracell clipping is absolutely avoided. The same holds for the IFFT processor.

In proceeding along the signal path the complex-valued signal is weighted by a complex coefficient \( w_{ilm} \) in the BFN. After each of the four real multiplications quantisation and (possibly) clipping is performed as indicated in Fig. 4 (wordlength \( w_B \), saturation level \( S_z \)).

Note that BFN clipping \( (N_{B}, N_{O}) \) is expected to occur so rarely in compliance with the considerations of chapter 2 that it is not taken into account in the sequel.

Signal wordlengths (being all fixed-point) are related to the associated saturation levels \( S_z \) according to [12]:

\[
q_s = S_z \cdot 2^{-w_{ilm} + 1}, \quad \xi = 1,2,3
\]

with \( q_s \) representing the quantisation step size. Quantisation is performed by (mathematical) rounding. Related noise spectra are considered white. All aliasing, quantisation and clipping noise contributions generated in a DEMUX-BFN system as shown in Fig. 4 are assumed uncorrelated with each other.

### 3.1. Aliasing distortion \( N_A \)

The aliasing power of stage \( \kappa \) is given by:

\[
N_A^\kappa = \frac{2^\xi}{M_F} \cdot M_P \cdot P \cdot 10^{-q_s/10}, \quad \kappa = 1, \ldots, 4
\]

where according to (4) \( M_P \) is the overall power of the adjacent slot (B) which is aliased to the usable slot under consideration. Actually, the aliasing contribution is diminished by the common UNDIFICE attenuation \( a_s \) (dB). Furthermore, the co-factor \( M_B^\kappa / M_F \) accounts for BFN misadjustment related to aliasing. From (12) the total aliasing distortion to be introduced into (3) readily follows:

\[
N_A = N_A^2 = \sum_{\kappa = 1}^{4} 2^\xi N_A^\kappa = 4N_E^2 \cdot \gamma^8 \cdot M_B^\kappa / M_F \cdot 10^{-q_s/10}
\]

where \( \gamma^8 \) obviously represents the amplification of \( N_A^\kappa \) introduced at output of stage \( \kappa \) up to the DEMUX output port. According to (8) we have \( \gamma^8 = L \), which is always used subsequently.

### 3.2. Quantisation noise \( N_Q \)

Intercell and I/O quantisation noise contributions transferred to the DEMUX output port and related to slot spacing \( B \) are given by [4,5]:

\[
L_{\mu}^{-2\xi} N_{E}^\kappa = 2L_{\mu}^{-2\xi} \cdot \frac{B}{f_s^\kappa / 2^\xi} \cdot \frac{q_s^2}{12}, \quad \kappa = 0, \ldots, 4
\]

where use is made of (1) and (8). Note that each (complex) signal has two components calling for the factor of 2 in (14).

Similarly, intracell quantisation noise is determined \((n_i; \text{ length of UNDIFICE})::\)

\[
L_{\mu}^{-2\xi} N_{E}^\kappa = 2L_{\mu}^{-2\xi} \cdot \frac{B}{f_s^\kappa / 2^\xi} \cdot \frac{n_i + 1}{2} \cdot \frac{q_s^2}{12}, \quad \kappa = 1, \ldots, 4
\]

In (15) it is anticipated that multiplication by \( c_0 \) does not contribute to quantisation noise, since
\[ c_0 = \gamma h_0 / \sqrt{2} = h_0 = 1/2 \text{ due to (8) and } w_1 > w_p; \text{ cf. Fig. 3 and [4,5].} \]

For the complex multiplication of BFN weighting we get in compliance with Fig. 4 and \( f_{\text{so}}^2 = 2B \):

\[ N_b = 4 \frac{B}{f_{\text{so}}^2} \frac{q^2}{12} = 2 \frac{q^2}{12} \] (16)

and at the BFN output port:

\[ N_{\text{m}} = 2 \frac{B}{f_{\text{so}}^2} \frac{q^2}{12} = 2 \frac{q^2}{12} \] (17)

Combining non-coherently all terms of (14) to (17) transferred to the BFN output port results in

\[ N_Q = \frac{N_E}{3} \left( 5 \cdot 2^{-2w_F} + 4 \frac{n_r + 1}{2} \cdot 2^{-2w_i} + 2S_2 2^{-2w_B} \right) + \frac{S_3^2}{3} \cdot 2^{-2w_m} \] (18)

to be introduced into (3), where \( S_2 = 2, S_3 = 8 \) and use is made of (11).

3.3. Clipping noise \( N_C \)

As a consequence of (8) and the discussion in section 2, clipping will only occur at the DEMUX input limiter (e.g., in conjunction with A/D conversion) and at the output ports of each UNDIFICE.

The model-based analysis of clipping noise is carried out according to [7,8] anticipating normally distributed signals. For the real and imaginary components of the complex FDM signal at DEMUX input, this assumption is valid, since many (QPSK, sinusoidal) signals are superimposed in a random manner [7]. However, at all other clipping points the tails of the distributions are somewhat modified as a consequence of clipping in preceding stages. Finally, it can easily be shown that simultaneous clipping of the real and the imaginary components of a complex signal within the DEMUX-BFN is very unlikely to occur.

The various clipping noise contributions to the real or imaginary component of a signal (Fig. 4) are estimated as a function of the peak factor \( p_f \) [7,8]:

\[ N_C = N_0, \quad \kappa = 0, \ldots, 4 \] (19)

where

\[ N_0 = \frac{2}{p_f^2 - 2} - \frac{2}{p_f^2} \phi(p_f) - \frac{2}{p_f^2} \phi(p_f) \times \left( p_f^2 - 3 + 2\phi(p_f) \right) \] (20)

and

\[ \phi(p_f) = \frac{1}{\sqrt{2\pi}} e^{-p_f^2/2} \] (21)

\[ \phi(p_f) = \int_{-\infty}^{p_f} \phi(x)dx \] (22)

Note that clipping noise is considered white for convenience. Thus we have at BFN output (non-coherent combination):

\[ N_C = 2N_EL \frac{B}{f_{\text{SI}}} N_0^0 + N_E^4 \sum_{\kappa=1}^{L} \gamma^{-2x} \frac{B}{f_{\text{SI}}^2/2^x} N_C^\kappa \] (23)

to be used in (3). In (23) at DEMUX input clipping is assumed both for the real and the imaginary component of the complex FDM signal, which is consistent with (5).

4. DEMUX design verification

Introducing eqs. (10), (13), (18) and (23) into SDR according to (3), and solving (3) for the UNDIFICE stopband attenuation calls for \( a_s > 42 \text{ dB} \) in order to achieve an SDR \( \geq 33 \text{ dB} \) for \( N_E = 10, \]

\[ L = 16, M_F = 3, M_F^2 = 2 [3], \text{ and } \gamma = \sqrt{2} \] under the condition of infinite precision signal processing. As a consequence the minimum filter length required is \( n_f = 11 \) approaching \( a_s = 56 \text{ dB} \) with unquantised coefficients [6].

Next, we look for an efficient UNDIFICE implementation suitable for VLSI. The approach adopted is to replace multiplication by addition in
conjunction with hardwired shifting: canonical signed digit (CSD) code \([9,10]\). The CSD code is a ternary code representing any coefficient with the smallest number of \(\pm 1\) terms. Because of \(\gamma = \sqrt{2}\) and \(n_t = 11\) only three UNDIFICE coefficients remain to be quantised (cf. Fig. 3 with \(c_0 = 1/2\)). Therefore, the CSD code coefficients that are globally optimum for a certain computational burden can be found by direct search in the discrete CSD code coefficient space. Results are given in Table 2 in conjunction with the associated minimum value of intercell signal wordlength as prescribed by (3): The most efficient coefficient set \([c_1, c_2, c_3]\) consistent with the specification \(w_F = 8\) bit [3] possesses only 8 non-zero entries. Its prototype frequency response (real coefficients: \(a_i = 48.56\) dB, passband ripple \(\Delta a_{\text{pp}} = 0.065\) dB) is shown in Fig. 5 together with the associated infinite precision design.

The remaining UNDIFICE parameters can be read from the design charts of Fig. 6 (where reasonable BFN signal wordlengths are anticipated: \(w_B = w_m = 10\) bit): Intracell signal wordlength \(w_i\) and the peak factor \(p_f\). Figure 6 shows the required stopband attenuation \(a_s\) as a function of \(p_f\) for \(\text{SDR} = 33\) dB. When choosing the minimum \(w_i = 9\) bit all peak factors \(p_f \in (3.14, 4.65)\) are allowed, where the required \(a_s\) ranges below those 48.56 dB of the UNDIFICE to be implemented. Hence, the most efficient approach still leaves sufficient margin for level fluctuations. In this case a maximum \(\text{SDR} = 34.2\) dB is obtained for the optimum peak factor \(p_f = 3.6\).

Finally, simulation results are shown in Fig. 7 in connection with the system performance predicted by design (Fig. 6) for an UNDIFICE intracell signal wordlength of \(w_i = 9\) bit and mathematical rounding (r). Simulation well confirms the design results for higher peak factors (low input power), where

| ![Fig. 5. Attenuation of UNDIFICE prototype; solid: CSD code representation of coefficients; dashed: unquantised coefficients.](image1.png) | ![Fig. 6. UNDIFICE stopband rejection versus peak factor for SDR=33 dB; \(n_t = 11, w_F = 8\) bit, \(\gamma = \sqrt{2}; N_F = 10, M_F = 3, M_F^* = 2, w_B = w_m = 10\) bit.](image2.png) |
| ![Fig. 7. Signal to distortion ratio SDR as a function of the peak factor \(p_f\), slot 1 and 4, \(w_F = 8\) bit mathematical rounding, \(w_i = 9\) bit mathematical rounding.](image3.png) | ![Table 2 Evaluation of UNDIFICE CSD code coefficients; \(n_t = 11\)](table2.png) |
deterioration is governed by rear end re-quantisation. For clipping (lower peak factors), however, system analysis yields somewhat too pessimistic results. This is attributed to the fact that the assumptions of [7] for clipping noise modelling are exactly met at the DEMUX input ports only (i.e. a signal clipped once and re-processed is no longer normally distributed). In the range of maximum SDR the performance of slot 4 exceeds that of slot 1, since the various aliasing contributions of slot 4 are subjected to a higher average attenuation than those of slot 1.

5. Conclusion

The analysis, design and simulation of a digital 16-slot FDM demultiplexer was reported. The tree-DMUX for processing of complex-valued signals is part of and specified by a beamforming environment [1,3]; Fig. 1. Its features verified by simulation are consistent with [3]:

- \( n_f = 11 \) length of UNDIFICE (halfband) prototype [4,5]
- CSD code coefficient representation
- \( \gamma = \sqrt{2} \) UNDIFICE scaling factor
- \( w_F = 8 \) bit intercell and I/O signal wordlengths
- \( w_T = 9 \) bit intracell signal wordlength; rounding
- \( SDR \geq 33 \) dB for \( \rho_f \in (2.9,4.6) \)
- \( SDR_{\text{max}} = 34.6 \) dB
- \( \rho_f = 3.5 \) optimum/nominal peak factor

It should be recognized that with a stand-alone application of the DEMUX (characterised by \( N_E = M_e = N_F^f = 1 \)) SDR > 30 dB is still achieved.

The approach to simulation is detailed in [11]. A high-speed ASIC implementation of this DEMUX is expected to require less than 30 kgates according to preliminary estimations.

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References