POLYPHASE IMPLEMENTATION OF UNRESTRICTED FRACTIONAL SAMPLE RATE CONVERSION

Alexandra Groth and Heinz G. Göckler

Digital Signal Processing Group, Ruhr-Universität Bochum,
Universitätsstr. 150, D-44780 Bochum, Germany

ABSTRACT

A recently proposed block-processing approach to polyphase implementation of fractional sample rate conversion (FSRC) [1-4] is revisited and extended to rational factors $L/M$ with arbitrary $L, M \in \mathbb{N}$. For a $z$-domain derivation of this type of FSRC a novel multirate identity is introduced. Potential applications include parallelization of digital systems to any desired degree for minimum power consumption.

1. INTRODUCTION

In digital systems noninteger sample rate conversion performed by a fractional sample rate converter (FSRC) is one of the basic tasks. The system theoretic approach is a cascade connection of an $L$-fold upsampler, a filter $H(z)$ and an $M$-fold downsampler (Fig.1), where $H(z)$ combines anti-imaging and anti-aliasing filtering. Recently, various derivations of FSRC have been published [1-4] under the constraint that the resampling factor $R = L/M$ is represented by the ratio of two relatively prime positive integers. As a result, the block processing approach to FSRC according to Fig.1 is obtained [3], where filtering is completely performed in the $L \times M$ MIMO LTI subsystem at a fixed sub-nyquist rate.

In this contribution we want to overcome the above constraint and assume subsequently:

$$R = \frac{L}{M} = \frac{FL_0}{FM_0}; \quad L, M, F, L_0, M_0 \in \mathbb{N} \quad (1)$$

where $L_0$ and $M_0$ are coprime. Important applications can, for instance, be found in parallel implementations of ultra high speed or wideband multirate systems, where the decimation factor $M_0$ of the specified resampling factor $R = L_0/M_0$ is not consistent with the speed limitations of the semiconductor technology to be applied.

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Subsequently, we first introduce a novel identity for multirate systems in section 2, in order to derive the polyphase approach to unrestricted FSRC in section 3.

2. A NOVEL MULTIRATE IDENTITY

In the derivation procedure of the block processing approach to FSRC according to Fig.1 with coprime $L = L_0$ and $M = M_0$ [3], the noble identity [4] depicted in Fig.2 has widely been used.

However, for unrestricted FSRC with $L, M \in \mathbb{N}$ this noble
identity is no longer applicable and, hence, must be generalized. To this end we start from a cascade connection of an up- and a downsampler by $L = FL_0$ and $M = FM_0$, respectively, where downsampling is additionally delayed by $\mu$ time units with $\mu \in \mathbb{N}_0$ as shown on top of Fig.3.

From the original circuit of Fig.3 a first identical structure is readily obtained by separating the common factor $F$ from $L$ and $M$, respectively, in order to form a subsystem as indicated by the dashed box. According to [4] (application of polyphase identity) the output signal of such a subsystem is identically zero in case of $\mu \neq F\nu$ with $\nu \in \mathbb{N}_0$. Hence, in the following we assume $\mu = F\nu$.

\begin{align*}
\mu &= F\nu = lL - mM, & \text{Case a} \quad (2) \\
\mu &= F\nu = mM - lL, & \text{Case b} \quad (3)
\end{align*}

with $l, m \in \mathbb{N}_0$. By introducing these substitutions into the structure of Fig.3, the center delay can be split and allocated in part both at the input and the output of the structure, as depicted in Fig.3. As a result of the application of some basic noble identities including that of Fig.2, the structure depicted on bottom of Fig.3 is obtained.

Next we introduce some extra delay in the original arrangement of Fig.3, as shown in Fig.4 for Case a. The output delay $z^{-m}_0$ is required for feasibility of the second and third identity of Fig.3. The reason for the output delay $z^{-F-1}_0L_0$ will be explained soon. By replacing the cascade connection of upsampling by $L$ and subsequent delayed downsampling by $M$ of Fig.4 (top) with the final identity of Fig.3 (bottom), it is possible to shift the output delay $z^{-F-1}_0L_0$ in front of the output upsampler by $L_0$ (first identity of Fig.4). Note that $z_0 = z^{-M}_0 = z^{-M}_0$.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Fig4.png}
\caption{Steps to derive the novel identity (Case a)}
\end{figure}

In the next step (second identity of Fig.4), the delay $z^{-F-1}_0L_0$ is equivalently substituted with a delay chain - perfect reconstruction (DC-PR) system [4] with $F$ branches for down- and upsampling by $F$. By shifting the $M_0$-fold downsampler and the $L_0$-fold upsampler into each branch of the DC-PR system and subsequent combination with down- and upsampling by $F$, respectively, the finally desired structure is obtained (third identity of Fig.4). Note that by the shifting operations the delay chains are now related to the input and output rates of the system, respectively.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Fig5.png}
\caption{Novel multirate identity for Case b}
\end{figure}

In Case b the same derivation procedure can be applied yielding the identity depicted in Fig.5. Here, in contrast to
Case a, an extra delay according to \( z_i^{-(F-1)M_0-l} \) has been added, where \( z_i^{-(F-1)M_0} = z_o^{-(F-1)L_0} \).

3. UNRESTRICTED POLYPHASE FSRC

For the development of the approach to unrestricted FSRC, we henceforth assume \( L \geq M \) in order to be specific. To this end we decompose the cascade combination of \( H(z) \) with subsequent downsampling by \( M \), the output decimator of the system theoretic approach to FSRC according to Fig.1, into \( M \) polyphase components:

\[
H(z) = \sum_{\mu=0}^{M-1} z^{-\mu} H_\mu(z^M)
\]

(4)

The resulting structure, obtained by exploiting a basic noble identity, is depicted in Fig.6. (We could also have decomposed the input interpolator of Fig.1 into \( L \) polyphase components which, however, had been more suitable in case of \( L < M \) [3].)

![Figure 6: Polyphase decomposition of output decimator of the system theoretic approach to FSRC (\( L \geq M \))](image)

Our ultimate goal is to develop a block processing structure for FSRC as shown in Fig.1. Therefore, the next intermediate step is to reverse the order of up- and downsamplers in Fig.6. For this purpose upsampling by \( L \) and all delays of the delay chain are shifted into the \( M \) branches of the polyphase structure of Fig.6. As a result, any branch \( \mu \) comprises an upsampler followed by a \( \mu \) time units delay \( z^{-\mu} \), a downsampler and the branch filter \( H_\mu(z) \). Next, those cascade combinations in front of the branch filters are replaced with the multirate identity according to Fig.4, as shown in Fig.7 (Obviously, \( L_0 = 0 \)).

![Figure 7: Order reversal of upsampler and downsampler with zero-branches discarded](image)

It should be noted that, in Fig.7, two features of the systems according to Fig.4 have implicitly been exploited. The first property is due to the fact that for all \( \mu \neq F \nu \) (\( \nu \in \mathbb{N}_0 \), \( F \in \mathbb{N} \): common factor of up- and downsampling) the transfer functions of the structures of Fig.4 are identically zero. Hence only those branch filters with \( \mu = F \nu \) are retained in Fig.7. Secondly, by the above substitution some extra delay, \( z_o^{-(F-1)L_0} \) and \( z_o^{-m} \) is introduced. The former is identical for all \( \mu \), whereas the latter depends on \( \mu \), being subsequently accounted for by the substitutions \( m := m_\mu \) and \( l := l_\mu \), respectively, in Eq.(2) and (3). However, in order to retain the FSRC system magnitude response, the overall delay introduced must be identical for all branches. For this reason, a branch dependent supplementary delay given by

\[
z_o^{-a_\mu} = z_o^{-l_\mu + \nu f / F} z_o^{-m_\mu}
\]

(5)

is combined with the branch filters, where \( \mu = F \nu \). According to [3] the first term of Eq.(5) represents the minimum additional delay for system realizability. Since this first term already comprises the delay \( z_o^{-m_\mu} \) introduced by the novel identity (Fig.4), it must be compensated for by the second term of Eq.(5).

For a third rearrangement step note that the structure of Fig.7 represents an \( M \)-branch polyphase system, where obviously always \( F \) branches have a common branch filter (\( M = F M_0 \)). Since \( L_0 \) and \( M_0 \) are coprime, \( l_\mu \) assumes each value of the set \([0, \ldots, M_0-1]\) for \( \mu = F \nu \) and \( \nu = 0, \ldots, M_0-1 \) (one-to-one mapping property of Euler Theorem). Hence, by suitably combining the delays \( z_i^{-l_\mu} \) with the delays \( z_i^{-m_\mu} \) of the \( M_0 \) identical input delay chains of the novel \( F \)-branch identity of Fig.4, the front end of the structure of Fig.7 is rearranged to the familiar form of an
In the last step of rearrangement, the $M$-branch input blocking circuit for decimation by $M$. In order to obtain the reordered system depicted in Fig.8, in addition, the $M_0$ output branch filters of Fig.7 are shifted into the respective paths of the novel $F^*$-branch multirate identity of Fig.4. Using the branch index $\kappa = 0, 1, ..., M - 1$ the $M$ branch filters are defined by

$$G_\kappa(z_o) = H((\kappa)_{M_0})_{\kappa}(z_o),$$  \hspace{1cm} (6)

where $(x)_y = x$ modulo $y$. Obviously, the modulo operation $(\kappa)_{M_0} = l_{\mu}$ reflects the fact that each branch filter is part of the overall system $F$ times. Furthermore, according to Eq.(2) we have $\mu = (l_{\mu}L)_M = l_{\mu}L - m_{\mu}M$. Due to the output delay chains of the novel multirate identity the delay to be combined with the branch filters is increased according to

$$z_o^{-\beta_n} = z_o^{-(L_0(F - 1) - \alpha((\kappa)_{M_0})L)}$$ \hspace{1cm} (7)

In the last step of rearrangement, the $M$ output interpolators of Fig.8 for sample rate increase by $L$ (dashed blocks) are replaced by polyphase interpolators. As a result, we obtain $M$ polyphase interpolators with identical output unblocking circuits, which are merged into one by means of elementary signal flow graph identities [3] (Fig.9). The resulting $L \times M$ branch filters are defined by

$$z_o^{-\beta_n} G_\kappa(z_o) = \sum_{r=0}^{L-1} z_o^{-r} R_{\kappa,r}(z_o^L)$$ \hspace{1cm} (8)

where $z_o^L = z_s$ corresponding to subnyquist processing at $f_s$.

4. CONCLUSION

In extension to [3], a systematic $z$-domain based derivation of a minimal polyphase realization of fractional sample rate conversion by $L/M$ with arbitrary $L, M \in \mathbb{N}$ has been presented. Using a novel multirate identity, it has been shown that out of the $M$ polyphase subfilters of the structure of

![Figure 9: Polyphase implementation of FSRC; $L, M \in \mathbb{N}$](Image)

In contrast to [3], by free choice of $F$ it is possible to adapt the subnyquist operation rate $f_s = f_i/M = f_o/L$ of the FSRC system to any desired technology dependent clock rate.

5. REFERENCES


