A Per-Channel Transmultiplexer
Applying IIR Filters and
Logarithmic Processing

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ABSTRACT

This paper describes an extension of a recently published memory-oriented design for a digital transmultiplexer which performs conversion between TDM and FDM on a per-channel basis [2]. The processor uses a particular class of optimal IIR bandpass filters [5, 9] for interpolation (TDM-to-FDM) and decimation (FDM-to-TDM).

Hardware efficiency is obtained by implementing the transversal filter part in a logarithmic mode, wherein multiplication becomes addition. The low-order recursive filter part is separately realized and operates at the PCM sample rate in either direction. To guarantee stability under looped conditions [8], wave digital filters [17] are used for the implementation of the recursive filter part.

I. Introduction

During the past decade, numerous architectures for digital transmultiplexers (DTM) have been proposed [1]. Deviating from all approaches known so far, most recently an implementation of a DTM on a per-channel basis was explored by Kurth et al. [2]. By virtue of its memory-oriented architecture applying logarithmic signal processing, the computational burden of this approach is substantially reduced while its highly regular (modular) structure is retained.

The basic principle of operation of this novel system is briefly recalled [2]. The input is, for instance, a 24-channel 1.544 Mbit/s PCM-line (Fig. 1). The DTM converts 12 of these 24 channels into a single bit-stream representing an FDM SSB group between 60-108 kHz. Subsequent D/A conversion and analog bandpass filtering produce the standard FDM group signal. In the FDM/TDM direction, the DTM performs reciprocal functions.

Fig. 1: DTM System block diagram (TDM/FDM)

Referring to Fig. 1, the digital interface circuit demultiplexes the TDM input into 24 individual voice frequency channels, each consisting of 8-bit companded PCM words occurring at an 8 kHz sample rate. An idealized spectrum of a typical channel is shown in Fig. 2a. Following the

Fig. 2: DTM TDM/FDM Spectra (a) Input, (b) BPF, (c) Shifted Input, (d) Channel Accumulator, (e) Analog FDM group

268

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interface circuit there are 12 individual interpolating digital bandpass filters operating at a 112 kHz sampling rate. The inputs to the even-numbered filters are the individual TDM channel signals which are sample-rate increased to the filter rate. In the passband of the post DAC analog BP filter, between 60-108 kHz (Fig. 2e), the digital bandpass filter selects the desired input signal harmonic. The filtering action is illustrated in Fig. 2b. The input signals of the odd-numbered filters have to be shifted by 4 kHz before bandpass filtering occurs (Fig. 2c) by means of sign alternators (Fig. 1) in order to obtain the desired spectral orientation at the channel accumulator (Fig. 2d).

The filter design reported in [2] is suboptimal in terms of filter degree. This is due to the fact that the digital minimum-phase FIR bandpass filters used are derived from linear-phase prototypes by reflecting those zeros outside the unit circle back inside the unit circle [3]. Therefore, we present two different filter design results leading to more efficient filter implementations. The first result is based on the design of optimal minimum-phase FIR filters according to [4]. The second method is based on the application of multirate IIR bandpass filters designed according to [5]. In order to guarantee stability under looped conditions [2, 6], the recursive parts of the latter design are implemented as wave digital filters (WDF [7]). To obtain an efficient filter realization, logarithmic processing is used throughout the transversal filter part as described in [2].

II. Design Results

As an example, two digital BPF with their passband placed in the range between 8-12 kHz were designed. As it can be deduced from Fig. 2, adjacent channel signals exhibit opposite spectral orientation with respect to each other giving rise to unnoticeable crosstalk only. Hence, the filter designs are based on the following constraints (CCITT Rec. G.792) leaving some margin for coefficient quantization:

- 0-3.4 kHz and 16.3-56 kHz: $a \geq 81$ dB
- 3.5-7.4 kHz and 12.3-16.2 kHz: $a \geq 70$ dB
- 8.3-11.4 kHz (passband): $-0.1$ dB to 0.1 dB.

Minimum-Phase FIR Filter [4]

These requirements are met with some additional margin by an optimal minimum-phase FIR filter of length 350. Since the sampling rate is increased by a factor of 1.4, only 25 taps with 14 cyclically varying coefficients must actually be realized for the implementation of this interpolation filter [2, 6]. The filter used in [2] is of length $43^3$ requiring 31 taps.

Minimum-Phase IIR Filter [5]

It is well-known [5, 9] that multirate filters can most efficiently be realized by using a particular class of IIR filter transfer functions, defined by

$$H(z) = \frac{N(z)}{D(z)} = \frac{1}{\sum_{k=1}^{M} b_k z^{-dk}}$$

Here, $d$ is the sample rate alteration ratio. An optimal bandpass filter design based on (1) results in a numerator of length $15^4$ with all zeros on the unit circle and a denominator of degree 7 consisting of only single, real poles. Thus, a multirate bandpass filter of Fig. 1 can be implemented as a cascade of an IIR filter operating at the PCM sample rate of 8 kHz and an FIR interpolator with 11 (hardwired) taps. The attenuation frequency response of a typical BPF is depicted in Fig. 3, and the associated passband group delay response is shown in Fig. 4.

Fig. 3: Theoretical attenuation frequency response of IIR bandpass filter (Channel 2)

Fig. 4: Theoretical group delay of IIR bandpass filter (Channel 2)
III. Implementation

In the telecommunication network a DTM is generally contained in the four-wire branch of a two-wire subscriber link. Thus, a DTM actually operates in a looped arrangement, yet stability has to be guaranteed under any adverse condition which may occur in practice [2, 6]. For our DTM approach with an inherently single-way modulation scheme, this kind of stability will be achieved if the following two (sufficient) requirements are met [6]:

- The (linear) loop gain must never exceed unity.
- The filters and networks used in the DTM must be completely stable, i.e. free of any parasitic oscillations [10].

These requirements can be met with an implementation of the IIR bandpass filter of Fig.1 as a cascade of a certain number of WDF's and an FIR filter realizing the numerator of (1), appropriate scaling provided [6, 10].

The proposed filter structure is shown in Fig.5. First, the incoming signal is expanded to linear format. Since all 7 poles of (1) are real, the denominator of the transfer function can be realized as a cascade of 7 WDF's of order 1. Two actual implementations of these filter blocks are depicted in Fig. 6, where $z_{in}$ indicates the pole location. Since all these blocks operate at the PCM sample rate of 8 kHz, the arithmetic operations including all measures for guaranteeing stability under looped conditions [6, 9] can easily be handled by a relatively simple signal processor. The resulting signal of the last 1st order block is converted to logarithmic number representation.

Subsequently, bandpass interpolation filtering is performed by an efficient memory-oriented FIR filter applying logarithmic processing as described in [5]. Thus, in each channel only 7 multiplications per input sample must be carried out.

![Diagram of WDF 2-port Adaptor](image)

$6s - 1 \ z_{in} > 0$

![Diagram of WDF 2-port Adaptor](image)

$6s - 1 \ z_{in} < 0$

IV. Conclusion

An extension of the transmultiplexer approach of Kurth et al. [2] with an inherently single-way modulation scheme has been described. In contrast to [2], IIR instead of FIR bandpass filters are applied leading to a substantially reduced number of arithmetic operations, as can be seen from Table I. Nevertheless, all desired features are retained, such as stability under looped conditions [6], a very low absolute value of the group delay (Fig.4), the absence of an additional analog frequency translation, and the application of logarithmic signal processing in the transversal part of the (noncanonic) IIR filter implementation.

Generally, a trade-off between numerator and denominator degree of (1) is required to find out the most efficient filter realization. If there are no hardware limitations, such as speed or power consumption, an optimally designed FIR filter according to [4] with logarithmic processing will usually be the best.
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<td>degree</td>
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<td>349</td>
<td>153</td>
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<td>26</td>
<td>11 + 7</td>
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<td>25 x 14, 350</td>
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Table I: Comparison of expenditure of three filter designs

choice, since it is highly modular [1]. If, due to hardware constraints, the maximum allowable numerator degree is too small to achieve a flat passband magnitude response, one will have to equalize the passband by a denominator polynomial of suitable order. This applies particularly to 60- or 120-channel DTM's requiring extremely high-order FIR filters. Hence, in these cases, the design of minimum-phase FIR filters becomes very difficult or even impossible.

Acknowledgment

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REFERENCES


